LISTING OF CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

1. (currently amended): A particularly configurable processor for processing error induced computer programs which are selectively operable on said particularly configurable processor, comprising:

~~a programmable~~ an error correcting circuit being programmable;

an instruction buffer for receiving instructions for microprocessor execution memory location for storing an error correction key; and

the error correcting circuit controlled at least in part by said error correction key, wherein the control of the error correction circuit permits correction in a predictable manner of intentionally inserted errors in a compiled program provided for execution in accordance with [[an]] a programmed error correction scheme ~~selected~~.

2. (canceled).

3. (original): The processor of claim 1, wherein said key enables selection of error correction specific to the induced error scheme.

4. (original): The processor of claim 1, wherein information provided in compiled computer program data in part controls said error correction, thereby providing complementary error correction with a combination of the error correction key and the information provided in the compiled computer program data.

5. (original): The processor of claim 4, wherein the key includes bits expandable into a larger set of bits which control the instruction op code decoder, signal routing, and logic circuit reconfiguration.

6. (original): The processor of claim 1, wherein a serial number in ROM participates in the control of the programmable error correcting circuit.

7. (original): The processor of claim 1, wherein an output register for data results is provided, the output register able to contain both correct results and plausible wrong results.

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8. (original): The processor of claim 1, wherein:

program instructions are provided in a pipeline architecture;

an information key is established as instruction security commands at a plurality of steps in said pipeline architecture; and

an arithmetic logic unit (ALU) provides variability of logic circuits for execution of encrypted op codes or standard op codes that provide standard instruction op code operation types.

9. (original): The processor of claim 8, further comprising:

a plurality of reconfigurable logic circuits able to calculate results of execution of an instruction;

a plurality of logic circuits including provisions for accepting correct data operands and plausible wrong data operands; and

said plurality of the logic circuits including provisions for outputting correct results along with plausible wrong results.

10. (original): The processor of claim 8, further comprising:

the key providing a capability of re-allocating memory resources and register resources;

a serial number in ROM which participates in the allocation of logic circuits and routing of signals; and

the serial number used in combination with the key in providing said capability.

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11. (original): The processor of claim 1, wherein:

instruction key information is shared with a compiler, the instruction key information used by the compiler to encrypt standard instruction op codes into encrypted instruction op codes; and

the key is stored in more than one memory cell type including a Read Only Memory (ROM), an Electrically Erasable Programmable Read Only Memory (E^2PROM), and a Random Access Memory (RAM).

12. (original): The processor of claim 1, wherein:

an output register for data results provides a capability of providing data containing both correct results and plausible wrong results; and

the correct results are provided in word locations in the output register coordinated by the key.

13. (original): The processor of claim 1, wherein data and instructions provided to a computer via program information include an intentional introduction of errors which are correctable with error correction algorithms, said correction algorithms pre-selected according to the key.

14. (original): The processor of claim 1, wherein:

dependency validation codes received through the multiplexer of the instruction buffer are checked by logic circuits that depend on the key, so that incorrect validation bits provide an alarm.

15. (original): The processor of claim 14, wherein:

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upon receipt of said alarm, the interdependency checking logic writes an audit code and is capable of terminating program execution.

16. (currently amended): The processor of claim 1, further comprising:

logic for requiring network handshaking, the network handshaking further used to provide additional key information for continued operation.[[.]]

17. (previously presented): A microprocessor for processing computer programs which are selectively operable on selected ones of individual microprocessors, comprising:

an error correcting circuit;

a programmable feature on the error correcting circuit, providing a selectability in an error correction scheme to be performed by the error correcting circuit; and

a memory location for storing error correction information, whereby the stored error correction information controls the programmable feature, thereby permitting correction in a predictable manner of intentionally inserted errors in a compiled program provided for execution in accordance with an error correction scheme selected.

18. (previously presented): Method for processing computer programs selectively operable on one or more selected individual microprocessors, comprising:

providing an error correcting circuit;

storing error correction control information in the form of an error correction key, thereby selecting an error correction scheme for execution in accordance with the key;

compiling program instructions in accordance with the selected error correction scheme, thereby permitting correction in a predictable manner of intentionally inserted errors in a program provided for execution in accordance with the error correction scheme selected; and

controlling said error correction controlled in part by information provided in compiled computer program data, thereby providing predictable error correction with a combination of the error correction key and the information provided in the compiled computer program data.

19. (canceled).

20. (original): The method of claim 18, further comprising:

using reconfigurable logic circuits for calculating the results of execution of an instruction op code;

the calculation of results of the execution of an instruction op code including accepting correct data operands and plausible wrong data operands; and

outputting correct results along with plausible wrong results.

21. (original): The method of claim 18, further comprising:

providing program instructions in a pipeline architecture; and

establishing information keys as instruction security commands at a plurality of steps in said pipeline architecture, wherein an arithmetic logic unit (ALU) provides variability of logic circuits for execution of encrypted op codes or standard op codes that provide standard instruction operation types.

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22. (currently amended): The method of claim 18, further comprising:

providing a key shared with a compiler;

encrypting standard instructions with the compiler using the key; and

storing both correct results and plausible wrong results in an output register in word locations in the output register coordinated by the key.

23. (original): The method of claim 18, further comprising:

providing a key shared with a compiler;

encrypting standard instruction op codes with the compiler using the key;

providing data and instruction op codes to the computer via program information including an intentional introduction of errors which are correctable with error correction algorithms, said correction algorithms pre-selected according to the key and long instruction words; and

changing the correction algorithms on a periodic basis by codes hidden in the instruction op codes gathered into an instruction buffer.

24. (original): The method of claim 18, further comprising:

using logic for requiring network handshaking; and

further using the network handshaking to provide additional key information for continued operation.

25. (previously presented): Method for compiling computer programs selectively operable on selected ones of individual microprocessors in which the individual microprocessors include programmable error correction circuitry, the method comprising:

selecting an error correction scheme for execution;

providing error correction control information in the form of an error correction key;

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controlling said error correction scheme in part by information provided in compiled computer program data, thereby providing predictable error correction with a combination of the error correction key and the information provided in the compiled computer program data; and

compiling program instruction op codes in accordance with the selected error correction scheme, thereby permitting correction in a predictable manner of intentionally inserted errors in a program provided for execution in accordance with the error correction scheme selected.

26. (previously presented): Method for limiting operability of a computer program to selected ones of individual microprocessors, comprising:

providing error correction control information for use in executing the program;

compiling program instruction op codes with intentionally inserted errors correctable by use of said error correction control information; and

controlling error correction in part by information provided in compiled computer program data, thereby providing predictable error correction with a combination of an error correction key and the information provided in the compiled computer program data.